ABSTRACT OF THE DISCLOSURE

In order to reduce a test time for a synchronous type memory device, a compression circuit compresses a plurality of memory cell data which are inputted in a plurality of read registers provided for a data output terminal to 1-bit data. A bank selection circuit selects an output of the compression circuit of either a bank #A or a bank #B. A tristate inverter buffer passes the 1-bit compression data selected by the bank selection circuit in accordance with a test mode command signal. The data output terminal outputs compressed data of a plurality of bits of memory cells. Thus, it is possible to simultaneously determine pass/fail of a plurality of memory cells, thereby reducing the test time.